

# PRANALI SARATE

## Design Verification Engineer

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### SUMMARY

I am a dedicated Design Verification Engineer with over a year of experience in verifying complex hardware designs. My expertise includes programming in Verilog/VHDL, a solid understanding of digital electronics, and hands-on experience in verification methodologies. I thrive in challenging environments and am committed to continuous learning and professional development.

### EXPERIENCE

#### Design Verification Engineer

##### Capgemini engineering

07/2022 - 09/2023 Bangalore, KA

Capgemini engineering specializes in engineering and R&D services.

- Preparing and maintaining of specific documents and data like functional specifications, safety analysis reports, and safety verification plans
- Analyzed verification methodology and test plan for new design at the RTL block level
- Acquired a deep understanding of the architecture which combines enormous computational capability
- Worked with the RTL team to fix bugs, read specs and implement test plans, functional coverage points, monitors, scoreboards, sequencers and sequences
- Debugged functional errors in the RTL model using simulation tools and debug tools based on in-depth understanding of architecture and RTL design
- Experience with HDLs such as Verilog, System Verilog, and SVA
- Good understanding of ASIC design flow and DV methodologies
- Strong Fundamental in Digital Electronics. Experience with test bench design and implementation

#### Test Engineer

##### Dhoot Transmission Private Ltd

02/2021 - 07/2021 Ch.Sambhajinagar, MH

Dhoot Transmission is involved in power transmission components manufacturing.

- Supported laser printing operations, contributing to the production of power transmission components
- Deepened understanding of laser printing techniques and their application in industrial settings
- Worked on lean angle sensors crucial for motorbikes, especially in high-performance riding or racing scenarios

### EDUCATION

#### BTech (E&TC)

##### Dr.BATU, Raigad

08/2017 - 05/2021

#### Class XII

##### Rastramata Indira Gandhi, Jalna

01/2017 - 05/2017

#### Class X

##### S.B High School, Ranjani

01/2015 - 05/2015

### KEY ACHIEVEMENTS



#### Enhanced Verification Accuracy

Decreased RTL development errors by 25% through rigorous verification.



#### Accelerated Project Delivery

Completed AMBA AHB2APB project 20% ahead of schedule.



#### Optimized Debugging Efficiency

Reduced test bench debugging time by 30% using automation.

### SKILLS

Debugging	Linux	Python
Fundamental electronics	SPI	SQL
UART	Ubuntu	Verilog HDL
Vivado	Windows	Xilinx ISE
System Verilog	UVM	

### TRAINING / COURSES

#### Verilog(VHDL)

#### Python

#### System Verilog

#### UVM

#### SQL

#### Power BI

### PROJECTS

#### AMBA AHB2APB Bridge RTL design

Open source SOC bus protocol for communication between high performance and low power devices.

- Designed an AMBA AHB2APB Bridge for high performance buses to communicate with low power devices.
- Developed a standardized bridge connecting AHB and APB buses, ensuring effective communication between different IPs.

#### SPI Protocol

Synchronous serial communication interface specification.

- Created SPI (Serial Peripheral Interface) Protocol for short distance communication in embedded systems using Verilog.

#### UART Protocol

UART project featuring key components for effective asynchronous communication.

- Implemented UART communication protocol consisting of Transmitter, Baud Rate Generator, and Receiver sections using Verilog.

